In the Drawings

The Examiner objected to the drawings because the headings of Figs. 4 and 5 are mis-numbered. The Examiner indicated that Applicant' specification discloses a fuse latch circuit in Fig. 4 and a Reference Generator in Fig. 5 but that Fig. 5 actually depicts the fuse latch circuit and Fig. 4 depicts the Reference Generator. Accordingly, Applicants have renumbered Figs. 4 and 5 to accurately reflect the detailed description.

The Examiner also objected to Fig. 4 now (Fig. 5) as failing to comply with 37 CFR 1.83(a) because Fig. 4 failed to show every feature specified in the claims. The Examiner indicated the band gap current reference of claim 13 must be shown or the feature canceled from the claims. Applicants respectfully submit that the "Current Source Derived From Bank Gap Reference" shown in the upper left quadrant of amended Fig. 5 shows the electrical equivalent of the band gap current source as a diode connected PFET and an ideal current source. The resistor selection block 201 identified by the Examiner is shown immediately below the band gap reference circuit in amended Fig. 5. Applicants have also amended Fig. 5 to correct the descriptive text for the band gap circuit, i.e. "Current Source Derived From Band Gap Reference."

A proposed set of drawings is attached as Appendix A to this amendment to overcome the Examiner's objections. Following the Examiner's approval of the form of the proposed drawings, Applicants will submit a formal set of drawings that will comply in all respects with 37 CFR 1.83 and 1.121.

Remarks

Claims 1-20 are pending in this action. Claims 1-11, 13 and 18-20 stand rejected. Claims 12 and 14-17 are objected to. By this amendment, claims 6, 7, 9, 11, 14, 15 and 18 have been amended and reconsideration of all pending claims herein is respectfully requested.

Claim Objections

The Examiner objected to claim 6 as having insufficient antecedent basis for the limitation "said fuse element." Applicants have amended claim 6 to recite an anti-fuse element coupled to the latch device. Therefore, Applicants have overcome the Examiner's objection to claim 6.

The Examiner objected to the recitation in claim 13 of a band gap current reference, indicating the disclosure does not teach a device called a band gap current reference. As noted above, Applicants have corrected a typo in the descriptive text of amended Fig. 5 to recite a "Current Source Derived From Band Gap Reference." Therefore, Applicants have overcome the Examiner's objection to claim 13.

The Examiner objected to claims 12 and 14-17 as being dependent upon a rejected base claim, but indicated claims 12 and 14-17 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Accordingly, Applicants have amended claim 15 to include all the limitations of independent base claim 1 and made claims 11 and 14 dependent on claim 15. Therefore, Applicants have overcome the Examiner's objection to claims 12 and 14-17.

Claim Rejections - 35 U.S.C. § 102(b)

The Examiner rejected claim 18 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,384,666 to Bertin, et al., stating that Bertin discloses a latch device with a variable resistive trip point and current source that compensates for variations in manufacturing and

operating environments. Applicants respectfully submit that Bertin is directed to a variable resistive trip-point latch where the current reference is adjusted for process, voltage and temperature (PVT) and this reference current is applied to a fuse to develop a diagnostic voltage across the fuse element to in turn derive an accurate trip point voltage based on the device geometries of the fuse latch. However, Bertin does not teach the element of compensating the reference current level for variations in the fuse latch trip point caused by variations in PVT. As such, the structure and method taught by Bertin does not anticipate Applicants' invention herein.

Applicants respectfully submit that drifting of trip point voltage in a fuse latch caused by PVT variations is a distinct technical problem not addressed by Bertin, which varied the current flowing through the latch circuit to vary the fuse resistance to achieve a predetermined trip point voltage. (Bertin, Col. 8, lines 15-24) Applicants note that the variable resistive trip-point latch of Bertin senses an "open" fuse when the fuse voltage is above the trip point of the fuse latch and senses an "intact" fuse when the fuse voltage is below the trip point of fuse latch. (Col. 8, lines 47-60) In this context "Fuse voltage" describes the voltage generated across the *fuse* by the current reference, which is a function of fuse resistance and ultimately used as a reference to determine the state of the fuse. (Col. 8, lines 26-32)

Not addressed by Bertin is the problem of trip point voltage drift caused by changes in operating characteristics of the devices comprising the fuse latch. For example, at elevated operating temperatures the relative drive strength of PFET devices increase while the drive strength for NFET devices decrease with temperature. Such an imbalance in relative drive strength of PFETs and NFETs within the fuse latch can lead to variation in the trip point voltage of the fuse latch. Consequently, it is desirable to adjust the voltage applied to the fuse during the sense operation to compensate for the variation in trip point voltage experienced by the fuse latch so the state of the fuse may be reliably sensed and saved in the fuse latch.

Applicants note the variable resistive trip point latch of Bertin is achieved by varying the current through the latch circuit to the fuse element during a sensing operation, such that the amount of fuse resistance required to generate a sufficient voltage to trip the fuse latch is varied. (Col. 8, lines 17-24) In Bertin, the current supplied to the fuse has been made immune to changes

in PVT for the purpose of making the fuse voltage ***constant*** to ensure reliable initial resistive evaluation and correct reading of the fuse state. However, Bertin does not modify the reference current to compensate for trip point voltage drift of the fuse latch due to variations in PVT. As a result, the latch trip point will vary with fluctuations in PVT, resulting in a higher margin of measurement error when sensing the state of a fuse element.

Conversely, Applicants in Fig. 5 of the pending application disclose a mimic device 202 that outputs the trip point of the inverter-latch coupled to the fuse-latch in Fig. 4. The corresponding output voltage "VREF" is an input to a differential amplifier 203, which compares the "VLAT" input to "VREF" and calculates the current control level "VSWITCH" that will make the VLAT level equal to VREF at a predetermined resistance level. Applicants respectfully submit that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described in a single prior art reference. MPEP §2131. Here, Bertin does not anticipate Applicants' claimed invention because Bertin does not teach compensating the reference current level for variations in the fuse latch trip point voltage caused by PVT parameters. To more clearly define and distinctly claim the invention, Applicants have amended claim 18 to include a limitation regarding a compensated current source adapted to adjust for variation of the fuse latch trip point voltage and also recite additional circuitry to enabling the invention. Therefore, Applicants respectfully submit that the Examiner's rejection of claim 18 under 35 U.S.C. § 102(b) has been overcome and claim 18 is condition form allowance.

Claim Rejections - 35 U.S.C. § 103(a), first paragraph

The Examiner rejected claims 1, 11, 19 and 20 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,892,716 to Ingalls in view of U.S. Patent No. 5,289,412 to Frary. The Examiner indicated that Ingalls discloses a latch device with a variable resistive trip point and a control element to vary the amount of current passing through the latch circuit based on the adjustable trip point. The Examiner further stated that Frary teaches circuitry for checking the condition of a memory cell, where a mimic circuit is used for compensation. The Examiner stated that it would have been obvious to one of ordinary skill in the art to combine Ingalls with Frary by placing a device matching the impedance of the latch circuit in series with the current

reference and latch circuit for providing a high performance sensing operation.

Applicants respectfully submit that Ingalls is directed to testing of an impedance of a programmable fuse element without compensation for PVT parameters. For example, Fig. 4a of Ingalls depicts a latch circuit wherein a margin test is implemented by turning on an additional finger device 122 of the current supply element 120. The configuration shown in Ingalls provides a 2-level binary resistive trip adjustment, Applicants further submit that neither of these levels is predictable because elements 124 and 122 are turned on with full Vcc overdrive and are affected by PVT variations. In any case, Ingalls does not teach or suggest a means for PVT compensation nor is the need for fuse latch trip point compensation addressed by Ingalls. Accordingly, Applicants respectfully submit that Ingalls does not suggest or motivate compensating for PVT induced variations in the trip point voltage of a fuse latch.

Applicants respectfully submit that Frary teaches away from Applicants' invention because Frary is based on a fundamentally different storage technology. The Examiner states that memory cell elements are equivalent to latches and therefore it would have been obvious to combine the teachings of Ingalls and Frary. Applicants respectfully submit that only SRAM cells are equivalent to latch circuits and the memory cells disclosed by Frary are MOSFETs implemented in a non-volatile EEPROM flash memory (Frary, Col. 2, lines 55-68) rather than latch elements as claimed by Applicants. Nor does Frary teach distributing a current reference to a plurality of latch elements or provide circuitry for checking the condition of a latch circuit. Applicants respectfully submit that Frary discloses a current mirror to distribute a reference voltage across a memory array of EEPROM elements. Similarly, no motivation appears in Frary to use a short circuited inverter to predict the trip point of a latch using that inverter as claimed herein. Nor does Frary suggest using the voltage of a mimic latch to calculate a current needed to measure the resistance of an electrical fuse. As such, Frary whether in combination with Ingalls or standing alone does not suggest or motivate Applicants' claimed fuse latch with compensated programmable resistive trip point.

Accordingly, a prima facie case of obviousness has not been established because Ingalls in combination with Frary does not suggest or motivate the structure and method claimed by Applicants. Claims 2-10 depend from claim 1; claim 11 now depends from claim 15 as amended;

claim 13 depends from claim 1; and claim 20 depends from claim 19. Therefore, Applicants respectfully submit that the rejection of claims 1, 11, 19 and 20 under 35 U.S.C. § 103(a) has been overcome and that all claims are in condition for allowance.

Allowable Subject Matter

Applicants gratefully acknowledge the Examiner's indication that claims 12 and 14-17 would be allowable if rewritten to include the limitations of any base claim and any intervening claims. Accordingly, Applicants have amended claim 15 to include all the limitations of independent base claim 1 and made claims 11 and 14 dependent on claim 15.

Prior Art Made of Record

The prior art made of record by the Examiner and not relied upon, i.e. Ingalls (U.S. Patent No. 6,760,806 has been reviewed and Applicants respectfully submit that the reference cited does not anticipate or suggest the elements of pending independent claims 1, 15 as amended, 18 and 19, nor of pending dependent claims 2-17 and 20.

Conclusion

Based on the foregoing, it is respectfully submitted the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,
For: Darren L. Anand, et al.

By: Michael J. Le Strange

Michael J. Le Strange
Registration No. 53,207
Telephone No.: (802) 769-1375
Fax No.: (802) 769-8938
EMAIL: lestrang@us.ibm.com

International Business Machines Corporation
Intellectual Property Law - Mail 972E
1000 River Road
Essex Junction, VT 05452